

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

• Applicant: Leonard Forbes et al.  
Title: DEAPROM AND TRANSISTOR WITH GALLIUM NITRIDE OR GALLIUM ALUMINUM NITRIDE GATE  
Docket No.: 303.355US4  
Filed: June 18, 2001  
Examiner: Unknown

Serial No.: 09/883,795  
Due Date: N/A  
Group Art Unit: 2814

SEP 24 2001

Commissioner for Patents  
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

A return postcard.  
 Supplemental Preliminary Amendment (8 Pages).  
 A check in the amount of \$590.00 to cover the fee for additional claims as calculated below.  
 Clean Version of Pending Claims (8 pgs.).

If an additional fee is required due to changes to the claims, the fee has been calculated as follows:

CLAIMS AS AMENDED						
	(1) Claims Remaining After Amendment		(2) Highest Number Previously Paid For	(3) Present Extra	Rate	Fee
TOTAL CLAIMS	35	-	20	15	x 18 =	\$270.00
INDEPENDENT CLAIMS	7	-	3	4	x 80 =	\$320.00
[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED						\$0.00
TOTAL						\$590.00

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and  
please charge any additional required fees or credit overpayment to Deposit Account No. 19-0748

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 18<sup>th</sup> day of September, 2001.

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Amy Mates

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S/N 09/883,795

PATENT

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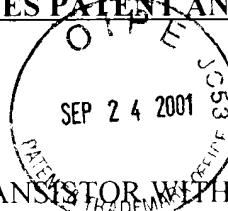
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SUPPLEMENTAL PRELIMINARY AMENDMENT

Commissioner for Patents  
Washington, D.C. 20231

Before taking up the above-identified application for examination, please enter the following amendments. Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set.

IN THE CLAIMS

Please amend the following claims and add claims 30- 61:

24. (Amended) A method of forming a floating gate transistor[, the method] comprising:  
forming a source region and a drain region[s] in a substrate;  
forming a gate insulator [from the gate insulator material] comprising silicon dioxide  
(SiO<sub>2</sub>) on a channel region in the substrate between the source region and the drain region; and  
forming a floating gate [from] comprising a floating gate material selected from the group  
consisting [essentially] of gallium nitride (GaN) and gallium aluminum nitride (GaAlN), such  
that the floating gate is isolated from conductors and semiconductors.

25. (Amended) The method of claim 24[,] wherein forming [the] a floating gate [includes]  
further comprises forming the floating gate by depositing the floating gate material by metal  
organic chemical vapor deposition (MOCVD).

26. (Amended) The method of claim 24[,] wherein forming [the] a floating gate [includes]  
further comprises forming the floating gate material by plasma-enhanced molecular beam epitaxy  
(PEMBE).

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02 FC:103

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